RDK X5 Module

Hardware Design Guide

Rev. 1.1

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
V1.0	2025-05-26	Initial release.
V1.1	2025-11-06	Merged ***RDK X5 Module datasheet*** Updated description. 1. Added 1.4 Key Features 2. Added 2.1.2 Module Output Reference Power 3. Added 2.2 Sleep Mode 4. Added 2.4 GPIO 5. Added Chapter 3 Mechanical 6. Added Connector PN. in 3.1 Connectors 7. Updated description

Contents

1 Introduction

1.1 Overview

The RDK X5 Module is equipped with the Sunrise 5 (X5) chip, which is a highly-integrated, high-performance and power-efficient artificial intelligence System-on-Chip (SoC) powered by D-Robotics.

Based on the Single-core BPU with Bayer-architecture, the X5 SoC supports real-time pixel-level video segmentation, structured video analysis and attention-based vision perception. The X5 SoC also integrates an Octa-core Cortex A55 CPU, one HiFi5 DSP which can support voice wakeup , an image signal processing (ISP) unit for wide/high dynamic range (WDR or HDR) and noise reduction (3DNR) in the camera input images processing, H.265/H.264/MJPEG video codecs, a 3D GPU supporting OpenGL ES 3.1/3.0 /2.0/1.1.

The RDK X5 Module integrates PMIC and DCDC chips, LPDDR4 and EMMC. The communication interface contains HDMI, Gigabit Ethernet, USB 3.0, MIPI CSI, and MIPI DSI. The module can be optionally equipped with a dual-band 2.4/5GHz wireless module, supports Wi-Fi 6 protocol and Bluetooth 5.4 protocol.

With the advanced toolkit provided by D-Robotics, RDK X5 Module can assist customers to achieve rapid mass production

1.2 Terms and Abbreviations

1.2.1 Terms & Definitions

Terms	Definitions
CSI	Camera Serial Interface
DSI	Display Serial Interface
MIPI	Mobile Industry Processor Interface
SPI	Serial Peripheral Interface
PWM	Pulse Width Modulation
LPWM	Light Pulse Width Modulation

1.2.2 Abbreviations

Abbreviations	Name
BPU	Brain Processing Unit
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AI	Analog Input

Abbreviations	Name
AO	Analog Output
AIO	Analog Input/Output
PU	Pull-Up
PD	Pull-Down
HSIO	High Speed Input/Output
LSIO	Low Speed Input/Output
AON	Always On
RTC	Real Time Clock
GPIO	General-purpose Input/Output

1.3 References Documents

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

RDK X5 Module Pinout Description and Application Note

RDK X5 Module Carrier Board

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the RDK X5 Module.

1.4 Key Features

- **Extensive Computing Resources**

X5 SoC integrates Octa-core A55 processors, 10Tops BPU, GPU and HiFi5 DSP.

- **Multi-camera inputs**

4×2lane or 2×4lane, up to 2.5Gbps per lane.

ISP Supports 4K@60Hz and maximum resolution of 4096x3072 pixels.

- **Rich Interfaces**

1×USB3.0 HOST, 1×USB2.0 DRD.

1×SD, 1×1000M PHY, 1×HDMI.

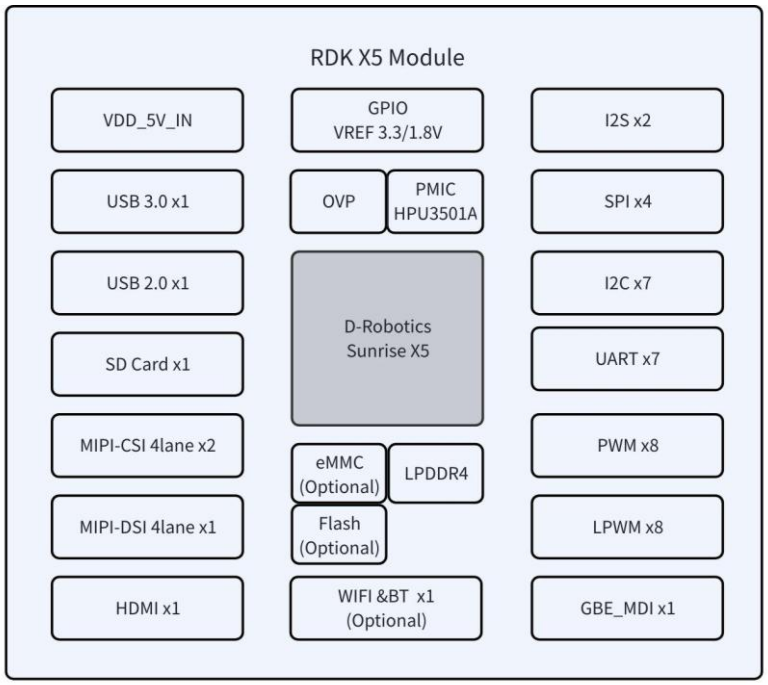
7×UART, 7×I2C, 4×SPI, 4×10bit ADC, 2×I2S, 1×2 channel PDM, 8×PWM, 8×LPWM.

Modules	Description
CPU	Octa-core Cortex A55, whose typical operating frequency is 1.5GHz L1 cache 32KB, L2 cache 64KB, L3 cache 1MB
BPU	Bayes architecture, up to 10Tops

Modules	Description
DSP	HiFi5 Audio DSP@812MHz
GPU	3D GPU, up to 32Gflops 2D GPU, support for multi-surface composition and 2D graphic processing
Memory	32-bit LPDDR4, up to 4266Mbps and 8GB address space. eMMC5.1, support for HS200 (optional) SD/SDIO3.0, support for SDR104 QSPI Flash, up to 100MHz (optional)
Video Input	MIPI CSI RX Multiple combination modes: 4x2lane or 2x4lane Up to 2.5Gbps per lane Support up to 4 Victual channel
Video Output	Support HDMI, 1080P@60fps Support 4Lane MIPI DSI TX, up to 2560x1440@60fps
ISP	Up to 4K@60fps Maximum resolution of 4096x3072 pixel Support 3D-NR, WDR, HDR, RGB-IR, PDAF
Video Codec	H264/H265, up to 4K@60fps ; MJPEG, up to 16M@30fps
Peripheral	1×USB3.0 DRD, 1×USB2.0 DRD 1×SD, 1×1000M PHY, 1×HDMI 7×UART, 7×I2C, 4×SPI, 4×10bit ADC, 2×I2S, 1×2 channel PDM, 8×PWM, 8×LPWM

1.5 Block Diagram

The following figure illustrates the overall design framework of the RDK X5 Module.



1.6 Pinout

The RDK X5 Module, featuring three independent connectors, offers 260 pinouts. These pinouts carry a diverse range of signals, including those for power supplies, cameras, displays, and Ethernet. In addition, it provides a flexible and extensive set of General-Purpose Input/Output (GPIO) pins. The RDK X5 Module supports multiplexing multiple functions on selected GPIO pins. For the specific pin definitions and usage guidelines, please refer to ***RDK X5 Module Pinout Description and Application Note***.

2 Hardware Design Recommendation

2.1 Power

2.1.1 Power Consumption

The RDK X5 Module integrates PMIC and DCDC chips, which means only 5V DC power is required to bring up the model.

- It is recommended to supply power to the RDK X5 Module with a minimum of 3A at 5V to ensure the stable operation of the module under maximum load.
- The Module is designed with a total of 11 VDD_5V_IN input power pins to supply power to the core module.

MD Pin No.	Signal Name	Description
77,79,81,83,85,87,249.251,253, 255,257	VDD_5V_IN	Power input: 4.75V-5.25V Main power input. Power input max 300mA per pin. RDK X5 Module requires at least 3A@5V.

NOTE:

Note that the RDK X5 Module has specific voltage requirements for the 5V supply.

1. The over-voltage lockout (OVLO) protection voltage is 5.25V.
2. The minimum operating voltage is 4.75V.

2.1.2 Module Output Reference Power

There are three kinds of power output pins on the RDK X5 Module:

- VDDIO18_DSP_UART
- MD_3.3V
- MD_1.8V

2.1.2.1 VDDIO18_DSP_UART

VDDIO18_DSP_UART is an always-on power, and remains powered in sleep mode. This pin is not designed for power supply. Please do not connect it on any load. Leave the pin unconnected if unused.

The power is only used to pull-up the following signals in the table below.

MD Pin No.	Signal Name	Description
248	AON_GPIO0_1V8	GPIO: Can be used for interrupt wakeup in sleep mode, internal 10KΩ pull-up to VDDIO18_DSP_UART.

MD Pin No.	Signal Name	Description
93	AON_FLASH_SLEEP_RESUME_N_1V8	GPIO: This Pin has multiple functions. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation.
222	AON_GPIO4_1V8	GPIO: Can be used for interrupt wakeup in sleep mode, internal 10KΩ pull-up to VDDIO18_DSP_UART.
234	Audio_IRQ_N_1V8	GPIO: Active-low interrupt request (IRQ) signal for audio-related events.
246	CODEC_I2S0_MCLK_1V8	GPIO: Master Clock signal for the I2S0.
242	CODEC_I2S0_DI_1V8	GPIO: Data Input line for the I2S0.
236	CODEC_I2S0_DO_1V8	GPIO: Data Output line for the I2S0.
238	CODEC_I2S0_SCLK_1V8	GPIO: Serial clock signal for the I2S0.
240	CODEC_I2S0_WS_1V8	GPIO: Word Select signal for the I2S0.
21	LED_SYS_STATUS_1V8	GPIO: Active-high output to control LED in the Carrier Board, which indicates that the running status of software. This pin is a switch control signal, cannot be used for driving a LED directly.
91	HOST_DIS_BT_N_1V8	GPIO: Driven low to disable the Bluetooth interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
89	HOST_DIS_WLAN_N_1V8	GPIO: Driven low to disable the wireless interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
68	DEBUG_UART0_RXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.
64	DEBUG_UART0_TXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.

2.1.2.2 MD_3.3V and MD_1.8V

MD_3.3V and MD_1.8V power off during sleep mode. These two power are typically used to supply power for GPIO_VREF on the carrier board. It is not recommended to drive the load directly.

2.1.3 GPIO VREF

The RDK X5 Module provides 31 GPIO pins (named XXX_VREF) with configurable voltage levels, which are determined by the GPIO_VREF (Pin 78).

- For 3.3V operation: Connect GPIO_VREF to MD_3.3V (pins 84 and 86).
- For 1.8V operation: Connect GPIO_VREF to MD_1.8V (pins 88 and 90).
- GPIO_VREF cannot be floating or connected to ground, otherwise the system will not work properly.

2.1.4 Peripherals Power

Typically the RDK X5 Module do not provide power supply for peripherals. Therefore, customer could design additional power sources such as 5V, 3.3V and 1.8V. Make sure that these power supplies should be powered up later than the system power supply.

It is recommended to use MD_3.3V and MD_1.8V as the enable of peripheral power supply.

NOTE:

1. If the peripheral device needs to keep working during sleep mode, it needs to provide an always on power. It means that MD_3.3V and MD_1.8V are not suitable for use as an enable signal under these conditions.
2. Be careful not to leak power from the peripheral GPIO port to the X5 SoC.

2.1.5 RTC Power

The RDK X5 Module supports the RTC (Real Time Clock) function, which is implemented based on the on-board PMIC. The backup power pin of the RTC is VRTC (Pin76), and the requirements are as follows.

- When using an external RTC battery, the voltage is required to be 2~3.3V, and its current discharge capacity should be greater than 2.5uA.
- The VRTC (Pin76) is connected in series with a 4.7KΩ resistor on the module for current limiting.
- When use rechargeable battery, the maximum charging voltage is required to be no less than 3.3V, and the maximum allowable charging current is required to be no less than 1mA.
- If the button cell battery is not rechargeable, a diode is needed to prevent charging of the battery.
- When the module is powered only by the RTC battery, it only supports counting and clock functions, and cannot wake up the X5 with an alarm.
- If do not need RTC function when the module is not powered on, let the VRTC (Pin76) keep floating.

2.2 Sleep Mode

The RDK X5 Module support configurable work modes to save power. In sleep mode, only the power domains of Always-On (AON), DSP Subsystem and DDR DRAM are active.

- In sleep mode, only VDDIO18_DSP_UART remains powered, MD_3.3V and MD_1.8V power off.
- In sleep mode, only Always-On (AON), DSP Subsystem and DDR DRAM are active, other external devices, such as the Ethernet, HDMI, Wi-Fi, Bluetooth, USB, MIPI Camera, cannot work.

- In sleep mode, only a part of the AON and DSP GPIOs remain operational. For details, please refer to 2.4 GPIO

2.3 System Control

The RDK X5 Module provides the following pins for system control-related purposes.

MD Pin No.	Signal Name	Description
160	EMMC_BOOT	Input: System startup control pin. Internal 100KΩ pull-up to MD_1.8V. Pull-down to ground via a 4.7KΩ resistor to boot from EMMC; leave floating to boot from NAND FLASH.
78	GPIO_VREF	Power input: GPIO voltage level selection for the pin named XXX_VREF. Must be connected to MD_3.3V (pins 84 and 86) for 3.3V voltage level or MD_1.8V (pins 88 and 90) for 1.8V voltage level. This pin cannot be floating or connected to ground.
89	HOST_DIS_WLAN_N_1V8	GPIO: Driven low to disable the wireless interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
91	HOST_DIS_BT_N_1V8	GPIO: Driven low to disable the Bluetooth interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
92	SYS_HW_RESET_N_1V8	Input: Driven low to reset the system. Internal 100KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
93	AON_FLASH_SLEEP_RESUME_N_1V8	GPIO: This Pin has multiple functions. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation.
99	GLOBAL_EN	Input: Driven low to power off the module. Internal 10KΩ pull-up to VDD_5V_IN.
100	RESETN_OUT_3V3	Output: An active-low reset output signal and generated by X5 module. The reset signal will be output in the following scenarios: hardware reset, software reset, watchdog timeout and entering sleep mode. Leave the pin unconnected if unused.
216	ADC_VINS7_RSVD	Input: The 7th ADC input channel, maximum input voltage of 1.8V. Reserved, this ADC is used for Carrier Board version identification.
21	LED_SYS_STATUS_1V8	GPIO: Active-high output to control LED in the Carrier Board, which indicates that the running status of software.

MD Pin No.	Signal Name	Description
		This pin is a switch control signal, cannot be used for driving a LED directly.
95	MD_LED_PWR_N_3V3	Output: Active-low output to drive Power On LED on the Carrier Board, which indicates that the X5 minimum system power-up is complete and reset is released. This pin is a switch control signal, not a LED sink current control signal. Cannot be used for driving a LED directly.

NOTE:

1. The state of EMMC_BOOT needs to match the design, otherwise there will be problems such as burning failed or boot failed. The EMMC_BOOT pin cannot be connected directly to ground.

EMMC_BOOT Pin Status	System Boot Device
NC, keep floating	NAND Flash
Pull-down to ground through a 4.7K resistor	eMMC

2. The RDK X5 Module provides two indicator light control interfaces (LED_SYS_STATUS_1V8 and MD_LED_PWR_N_1V8). Both interfaces are only for on-off control and cannot be used for driving a LED directly.
3. If MD_LED_PWR_N_1V8 is not used to indicate the power-on completion status, leave the pin unconnected if unused

2.4 GPIO

The RDK X5 Module provides multiple GPIO pins for general-purpose interfacing. According to the functional definition, they can be divided into the following categories:

- AON GPIO
- DSP GPIO
- High Speed GPIO (Such as SDIO)
- Low Speed GPIO (Such as SPI, I2C, UART)

2.4.1 AON GPIO

AON GPIO can be used in sleep mode. When the X5 Module enters sleep mode, connect wake-up interrupt signals (e.g. RTC alarm or push-button inputs) to AON GPIO pins. Make sure that each wake-up signal line must be pulled up to VDDIO18_DSP_UART (Pin 231).

The RDK X5 Module provides 3 AON GPIO pins.

MD Pin No.	Signal Name	Description
248	AON_GPIO0_1V8	GPIO: Can be used for interrupt wakeup in sleep mode, internal 10KΩ pull-up to VDDIO18_DSP_UART.

MD Pin No.	Signal Name	Description
93	AON_FLASH_SLEEP_RESUME_N_1V8	GPIO: This Pin has multiple functions. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation.
222	AON_GPIO4_1V8	GPIO: Can be used for interrupt wakeup in sleep mode, internal 10KΩ pull-up to VDDIO18_DSP_UART.

NOTE:

1. When using the sleep wakeup function, if the X5 chip is in sleep mode, the peripherals need to be powered to ensure that the peripherals can generate valid interrupt signals.

2.4.2 DSP GPIO

The RDK X5 Module provides 2 group DSP GPIO pins with different voltage standards. Among them, the DSP GPIO pins in the table blew can also be used in sleep mode, and the pull-up power should be VDDIO18_DSP_UART (Pin 231).

MD Pin No.	Signal Name	Description
234	Audio_IRQ_N_1V8	GPIO: Active-low interrupt request (IRQ) signal for audio-related events.
246	CODEC_I2S0_MCLK_1V8	GPIO: Master Clock signal for the I2S0.
242	CODEC_I2S0_DI_1V8	GPIO: Data Input line for the I2S0.
236	CODEC_I2S0_DO_1V8	GPIO: Data Output line for the I2S0.
238	CODEC_I2S0_SCLK_1V8	GPIO: Serial clock signal for the I2S0.
240	CODEC_I2S0_WS_1V8	GPIO: Word Select signal for the I2S0.
21	LED_SYS_STATUS_1V8	GPIO: Active-high output to control LED in the Carrier Board, which indicates that the running status of software. This pin is a switch control signal, cannot be used for driving a LED directly.
91	HOST_DIS_BT_N_1V8	GPIO: Driven low to disable the Bluetooth interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
89	HOST_DIS_WLAN_N_1V8	GPIO: Driven low to disable the wireless interface. Internal 10KΩ pull-up to VDDIO18_DSP_UART. Leave the pin unconnected if unused.
68	DEBUG_UART0_RXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.
64	DEBUG_UART0_TXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.

2.5 Function Interface Circuit Design

2.5.1 Ethernet

The RDK X5 Module integrates a Gigabit Ethernet PHY interface (RTL8211FS-VS-CG).

- 10/100/1000 Mbps Ethernet Transceiver.
- Support the Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE 1588 version 2 and IEEE 802.1AS.
- The Ethernet PHY operates in voltage-mode configuration.

2.5.1.1 Ethernet Interface Design

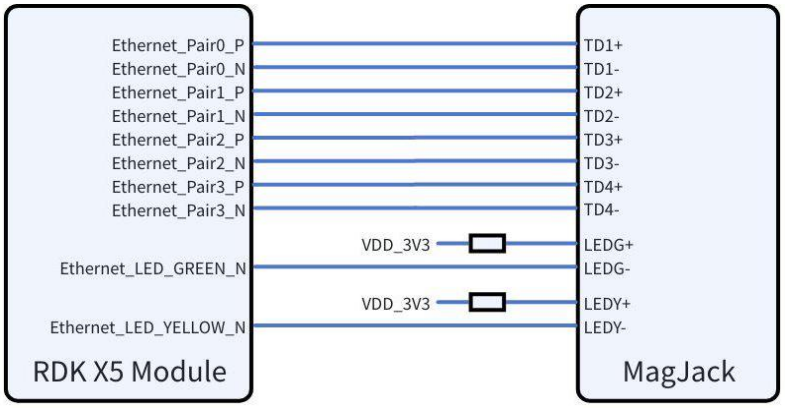
Ethernet interface includes the following pins.

MD Pin No.	Signal Name	Description
3	Ethernet_Pair3_P	Ethernet pair 3 positive (connect to transformer or MagJack)
4	Ethernet_Pair1_P	Ethernet pair 1 positive (connect to transformer or MagJack).
5	Ethernet_Pair3_N	Ethernet pair 3 negative (connect to transformer or MagJack).
6	Ethernet_Pair1_N	Ethernet pair 1 negative (connect to transformer or MagJack).
9	Ethernet_Pair2_N	Ethernet pair 2 negative (connect to transformer or MagJack).
10	Ethernet_Pair0_N	Ethernet pair 0 negative (connect to transformer or MagJack).
11	Ethernet_Pair2_P	Ethernet pair 2 positive (connect to transformer or MagJack).
12	Ethernet_Pair0_P	Ethernet pair 0 positive (connect to transformer or MagJack).
15	Ethernet_LED_GREEN_N	Output: Active-low Ethernet speed indicator, typically a green LED is connected to this pin. Internal 4.7KΩ pull-up to MD_3.3V.
17	Ethernet_LED_YELLOW_N	Output: Active-low Ethernet speed indicator, typically a yellow LED is connected to this pin. Internal 4.7KΩ pull-up to MD_3.3V.

NOTE:

1. The PHY provides two LED control interfaces (Ethernet_LED_GREEN_N and Ethernet_LED_YELLOW_N) for driving the status LEDs on the MagJack. The status LED turns on when the connected control pin is driven LOW.

Refer to follow figure for the connecting of MDI interface design.



2.5.1.2 Ethernet PCB Design

The following describes the layout recommendations for the MDI differential pairs

- Ensure that the length deviation of each pair of differential signal traces (MDI0+, MDI0−, MDI1+, MDI1−, MDI2+, MDI2−, MDI3+, MDI3−) falls within ±5 mils, and the impedance of the differential trace is 100Ω.

2.5.2 USB

The RDK X5 Module integrates dual USB ports: one USB 2.0 interface and one USB 3.0 interface. Both the 2 USB ports are natively implemented in the X5 SoC, requiring no additional USB hub circuitry in the design.

2.5.2.1 USB 2.0 Interface Design

The USB 2.0 port is designed as a Host/Device dual-role interface.

- Compatible with the Universal Serial Bus Specification, Revision 2.0.
- Support High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) mode.

USB2.0 interface includes the following pins.

MD Pin No.	Signal Name	Description
101	USB2_ID_3V3	Input: USB2.0 ID identify. Internal 10KΩ pull-up to MD_3V3. Driven low to change the USB2.0 to host role. Note that this GPIO cannot be used in the sleep mode.
103	USB2_D_N	USB 2.0 High-speed differential transceiver (negative).
105	USB2_D_P	USB 2.0 High-speed differential transceiver (positive).

NOTE:

2. By default, the USB 2.0 port operates in the device mode. In this mode, it supports several key functions such as firmware flashing, debugging, and virtual network card functionality.
3. Control the USB2_ID_3V3 can change the USB2.0 port role. The relationship between them is shown in the following table. Note that although USB2_ID_3V3 has a default pull-up on the board, the pin is output low state before the system starts up, which does not affect the judgment of the USB Role during system operation.

USB2_ID_3V3 STATUS	USB2.0 Role
NC	Devices
Pull-down	Host

4. When the USB is configured in host mode, the Carrier Board should have a dedicated power supply to the connector to power the peripherals, and carefully evaluate the problems of overload protection, power backflow, etc. For example: when the board is running and the USB is in host mode, the user incorrectly powers the USB port through the cable.

2.5.2.2 USB 3.0 Interface Design

The USB 3.0 port is designed as a Host/Device dual-role SuperSpeed interface.

- Compatible with Universal Serial Bus Specification, Revision 3.0.
- Support Super-Speed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) mode.
- Up to 5Gbps data rate.

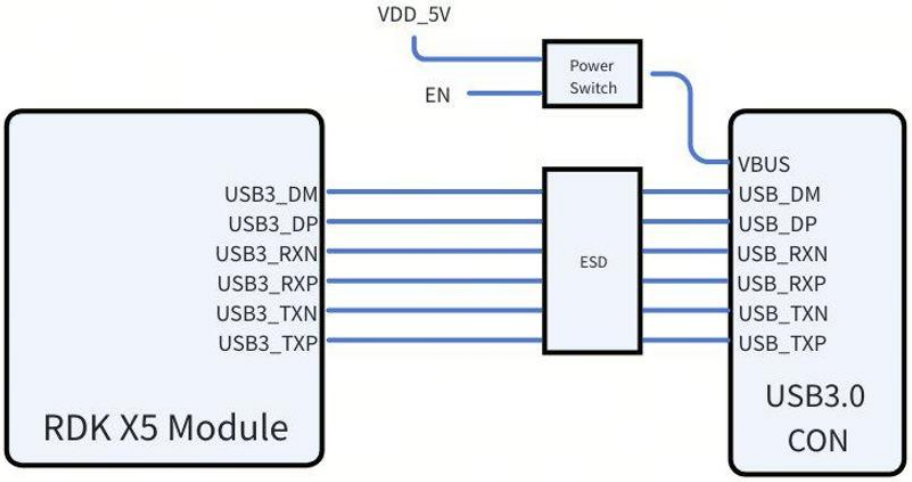
USB3.0 interface includes the following pins.

MD Pin No.	Signal Name	Description
157	USB3_RXN	USB3.0 Super-Speed receiver differential pair (negative).
159	USB3_RXP	USB3.0 SuperSpeed receiver differential pair (positive).
163	USB3_DP	USB3 High-speed differential transceiver (positive).
165	USB3_DM	USB3 High-speed differential transceiver (negative).
169	USB3_TXN	USB3 Super-Speed transmitter differential pair (negative).
171	USB3_TXP	USB3 Super-Speed transmitter differential pair (positive).

NOTE:

1. The 100nF AC coupling capacitors on the Super-Speed signals (USB_TX_P/N and USB_RX_P/N) have already been integrated inside the Module, so the AC coupling capacitors not need added on the Carrier Board.
2. By default, the USB 3.0 port operates in the device mode, and can be changed to host mode through software configuration.
3. In USB host mode, the board must have an external DCDC or Power Switch to supply 5V power to the USB connector.

Refer to follow figure for the connecting of USB3.0 interface design.



2.5.2.3 USB PCB Design

The following describes the layout recommendations for all the USB differential pairs: USB2_D_P, USB2_D_N, USB3_DP, USB3_DM, USB3_TXP, USB3_TXN, USB3_RXP and USB3_RXN.

Must be designed with a differential impedance of 90Ω.

- In order to minimize cross talk, it is recommended that each pair should meet the edge-to-edge 5W principle between differential signal pairs and other signals. Separating with ground as depicted will also help minimize cross talk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- In addition to the fan-out routing in the USB connector area, it is strongly recommended that the USB routing be on the inner layer and be well grounded.
- Signal vias cannot directly pass through the power plane. It is recommended to use GND to wrap the signal vias when passing through.
- USB routing should avoid the inductor projection area of the switching power supply. If necessary, a magnetically shielded inductor can be selected.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test point are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135°. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SuperSpeed differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces. There should be less than 5 mils difference between a SuperSpeed differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 25 mils relative trace length difference.

- The etch lengths of the differential pair groups do not need to match, but all trace lengths should be minimized.

Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible the module.

2.5.3 HDMI

The RDK X5 Module provides an HDMI output interface (SiI9022ACNU), which supports a resolution of up to 1080P at a frame rate of 60fps.

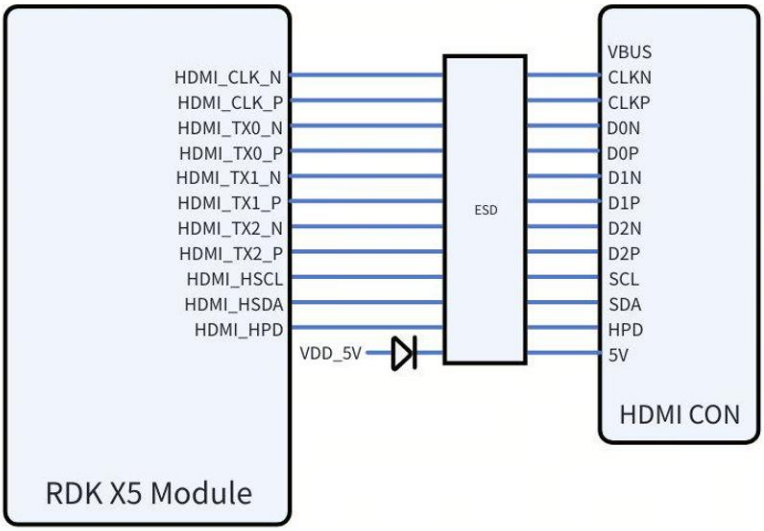
The HDMI interface is converted from the BT1120 interface of the X5 chip. The I2C address of HDMI transmitter is 0x76 on I2C7 of X5 SOC.

2.5.3.1 HDMI Interface Design

HDMI interface includes the following pins.

MD Pin No.	Signal Name	Description
153	HDMI_HPD	Input: HDMI hot plug Detect Input with 5V tolerant. It can be connected directly to the HDMI connector, an ESD protection and a 100KΩ pull-down resister need to be designed in the Carrier Board.
170	HDMI_TX2_P	HDMI TMDS output data TX2 positive.
172	HDMI_TX2_N	HDMI TMDS output data TX2 negative.
176	HDMI_TX1_P	HDMI TMDS output data TX1 positive.
178	HDMI_TX1_N	HDMI TMDS output data TX1 negative.
182	HDMI_TX0_P	HDMI TMDS output data TX0 positive.
184	HDMI_TX0_N	HDMI TMDS output data TX0 negative.
188	HDMI_CLK_P	HDMI TMDS output clock positive.
190	HDMI_CLK_N	HDMI TMDS output clock negative.
199	HDMI_HSDA	HDMI DDC I2C SDA. Internal 2KΩ pull-up to 5V. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the Carrier board.
200	HDMI_HSCL	HDMI DDC I2C SCL. Internal 2KΩ pull-up to 5V. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the Carrier board.

Refer to follow figure for the connecting of HDMI interface design.



2.5.3.2 HDMI PCB Design

The following describes the layout recommendations for the HDMI differential pairs.

- Ensure that the length deviation of each pair of differential signal traces falls within ±6 mils, and the impedance of the differential trace is 100Ω.
- Control 3 times line width between differential pairs, between differential and other signals.
- It is best to make several associated holes at the HDMI signal via to increase the return path.

2.5.4 MIPI

The RDK X5 Module supports both MIPI DSI and CSI protocols. In particular, the CSI interface of the RDK X5 Module is capable of accommodating up to four independent MIPI links, providing enhanced flexibility and expandability for various applications.

2.5.4.1 MIPI DSI TX Interface Design

The RDK X5 Module is compatible with the MIPI Alliance Interface specification v1.2, supporting 1 clock lane and up to 4 data lanes, with a maximum data rate of 2.5Gbps per lane.

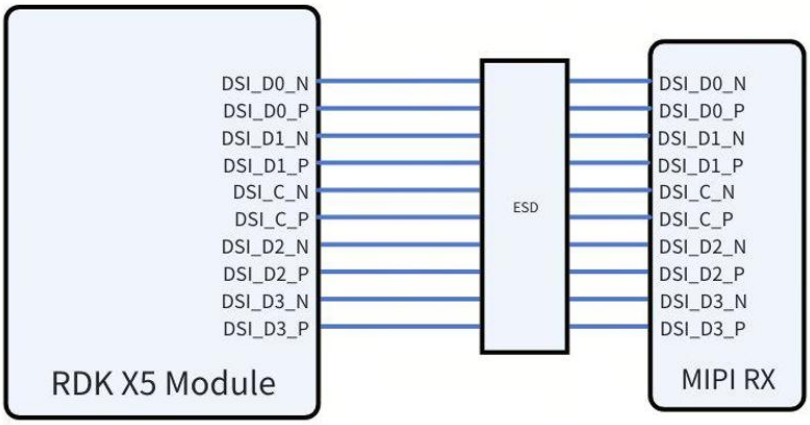
MIPI DSI interface includes the following pins.

MD Pin No.	Signal Name	MD Pin No.	Signal Name
175	DSI_D0_N	189	DSI_C_P
177	DSI_D0_P	193	DSI_D2_N
181	DSI_D1_N	194	DSI_D3_N
183	DSI_D1_P	195	DSI_D2_P
187	DSI_C_N	196	DSI_D3_P

NOTE:

1. When using MIPI DSI TX with 2 lanes, if configured by connecting DSI registers, only lanes 0 and 1can be used, and unused lanes can be floated.

Refer to follow figure for the connecting of MIPI DSI interface design.



2.5.4.2 MIPI CSI RX interface

The module is compatible with the MIPI Alliance Interface Specification DPHY V2.1. It supports up to 2*4 data lanes, with a maximum data rate of 2.5Gbps per lane.

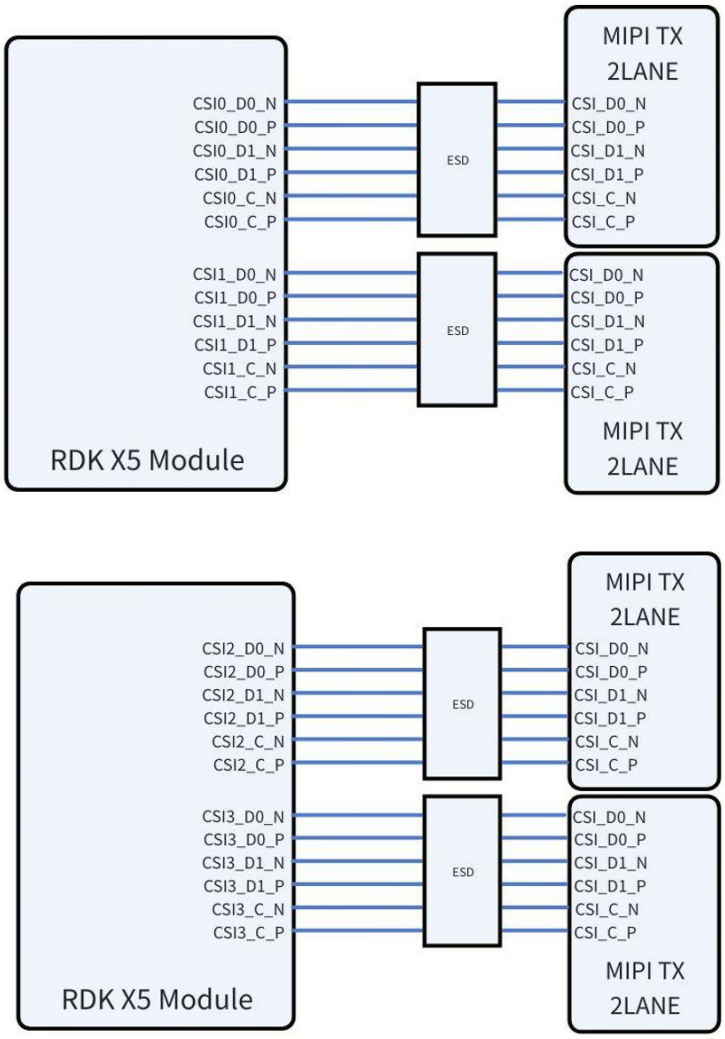
MIPI CSI interface includes the following pins.

MD Pin No.	Signal Name	MD Pin No.	Signal Name
127	CSI0_CLK_N	140	CSI2_CLK_N
129	CSI0_CLK_P	142	CSI2_CLK_P
115	CSI0_D0_N	128	CSI2_D0_N
117	CSI0_D0_P	130	CSI2_D0_P
121	CSI0_D1_N	134	CSI2_D1_N
123	CSI0_D1_P	136	CSI2_D1_P
152	CSI1_CLK_N	164	CSI3_CLK_N
154	CSI1_CLK_P	166	CSI3_CLK_P
133	CSI1_D0_N	118	CSI3_D0_N
135	CSI1_D0_P	116	CSI3_D0_P
139	CSI1_D1_N	124	CSI3_D1_N
141	CSI1_D1_P	122	CSI3_D1_P

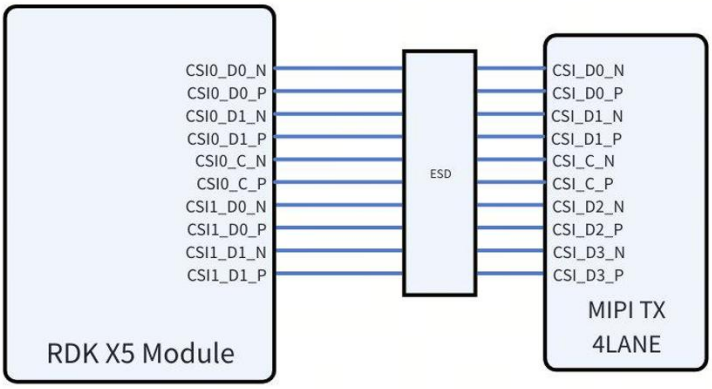
NOTE:

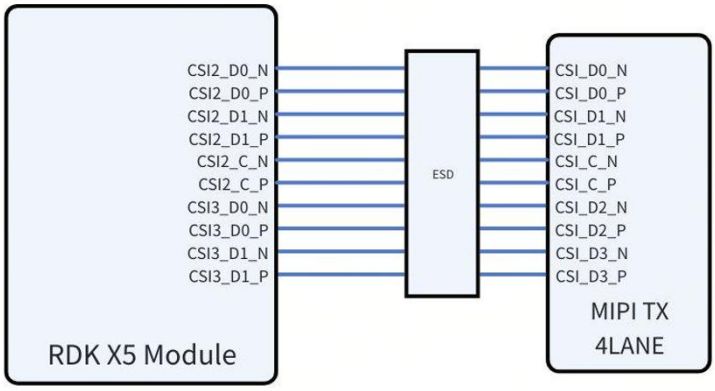
1. The CSI interface supports up to 4 MIPI RX links. In this case, each link has an independent differential clock and two data links. Additionally, the CSI interface supports combining 2-lane CSI configurations into a 4-lane CSI application.
2. The RDK X5 Module provides a rich set of GPIO outputs. When working with the default software driver, CAM1_EN_1V8 (Pin252) and CAM2_EN_1V8 (Pin256) are used for the enable and reset control of camera modules, adopting 1.8V digital logic. AON_GPIO1_3V3 (Pin97) is employed for the enable control of cameras with 3.3V digital logic.
3. For the default configuration of the camera I2C in software, please refer to the I2C section of this document.

The follow figure shows 2-lane mode in which all signals are connected point to point.



The follow figure shows 4-lane mode in which all signals are connected point to point.





2.5.4.3 MIPI PCB Design

The routing constraints are shown in the table.

NOTE:

When designing PCB, must import pin delay data on the RDK X5 Module from the Pin Delay sheet of *RDK X5 Module Pinout Description and Application Note. Due to the limitation of board size, MIPI signals are not strictly controlled in equal length on the module.*

Item	Design Rules
Zdiff	100Ω
Routing	■ The length difference between the signal P\N of the differential pair are within ±1ps ■ The delay difference of DATA from CLK are within +/-10ps ■ The signal length should be as short as possible. ■ MIPI routing should avoid the inductor projection area of the switching power supply. If necessary, a magnetically shielded inductor can be selected.
Spacing	■ The spacing between MIPI traces should meet the edge-to-edge 3W principle, which is applicable to the P/N within a differential pair and between differential pair groups. ■ If space permits and there is a reliable ground via design, it is recommended to insert GND traces between differential pair groups and between different CSI interfaces, which will help further reduce EMI and crosstalk between differential pair groups. It should be noted that the spacing between the GND trace and the signal trace should be kept consistent throughout, otherwise it may affect impedance control.
External calibration resistors	■ The routing length from external resistor to X5 CSI_REXT ball should be less than 5mm, and max parasitic

Item	Design Rules
	capacitance should be less than 2pF. ■ The routing length from external resistor to X5 DISP_DPHY_REXT ball should be less than 5mm, and max parasitic capacitance should be less than 2pF.

2.5.5 SD

The RDK X5 Module provides a single SD 3.0 host controller, which utilizes four-wire communication.

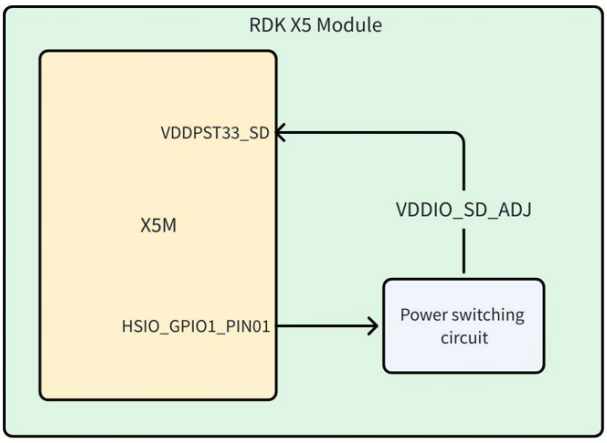
- It supports SDR12 at 25 MHz, SDR25 at 50 MHz, SDR50 at 100 MHz, and SDR104 at 200MHz.
- It is capable of adaptively supporting the two voltage level standards of 3.3V and 1.8V for SD cards.

SD interface includes the following pins.

MD Pin No.	Signal Name	Description
57	SDIO_TF_SCLK_ADJ	SD card clock signal.
61	SDIO_TF_DAT3_ADJ	SD card Data3 signal. Internal 47KΩ pull-up to VDDIO_SD_ADJ (SDIO IO Power Supply on the Module).
62	SDIO_TF_CMD_ADJ	SD card Command signal. Internal 47KΩ pull-up to VDDIO_SD_ADJ.
63	SDIO_TF_DAT0_ADJ	SD card Data0 signal. Internal 47KΩ pull-up to VDDIO_SD_ADJ.
67	SDIO_TF_DAT1_ADJ	SD card Data1 signal. Internal 47KΩ pull-up to VDDIO_SD_ADJ.
69	SDIO_TF_DAT2_ADJ	SD card Data2 signal. Internal 47KΩ pull-up to VDDIO_SD_ADJ.
258	SDIO_TF_CD_ADJ	SD Card Detect signal, when SD Card inserted, this pin should be high. Internal 47KΩ pull-up to VDDIO_SD_ADJ.

NOTE:

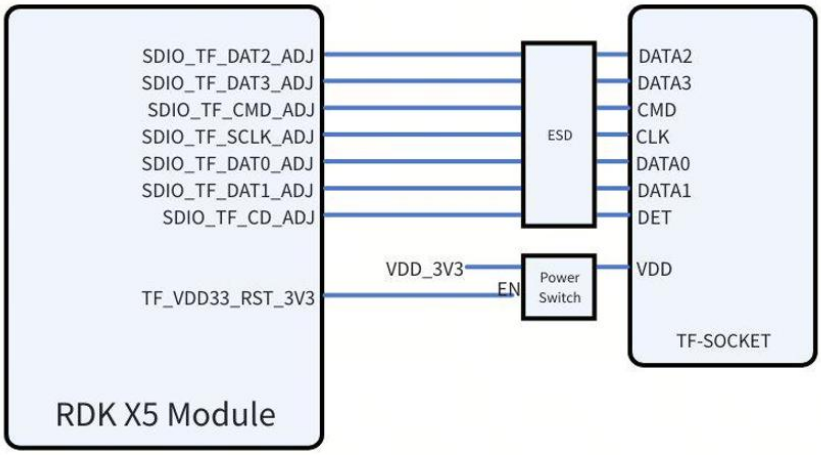
- VDDIO_SD_ADJ is the power domain of the SDIO signals. To comply with the SDIO protocol, VDDIO_SD_ADJ supports switching between 1.8V and 3.3V. This switching circuit is implemented on the Module, and the voltage level is controlled via HSIO_GPIO1_PIN01 in software according to the SDIO protocol. During power-on, VDDIO_SD_ADJ defaults to 3.3V. Therefore, it is strongly recommended to avoid using the SDIO signals for GPIO functions. If necessary, they should only be used as GPIO with 3.3V level, and HSIO_GPIO1_PIN01 must be set to output high.



- The module provides an SD card insertion detection signal named SDIO_TF_CD_ADJ. When a TF card is inserted, this pin should be at a high level. With default software configuration, a normal close switch type socket need be selected.
- The module offers a pin named TF_VDD33_RST_3V3 (Pin 75) for controlling SD card power supply, which is used to reset the SD card. In the case of using a Module without an on-board EMMC, the SD card will serve as the boot medium. In the design of the Carrier Board, this control pin must be set to a high level by default. It is recommended to pull it up to 3.3V through a 10KΩ resistor.

MD Pin No.	Signal Name	Description
75	TF_VDD33_RST_3V3	SD card 3.3V power supply enable signal. Output high level to turn on the SD card power switch on the Carrier Board. Internal 10KΩ pull-up to MD_3.3V.

Refer to follow figure for the connecting of SDIO interface design.



2.5.5.1 SD PCB Design

The design requirements on the SDIO signals are as follows:

- Ensure that the spacing between adjacent signal traces complies with the center-to-center 3W rule. Wider spacing between traces helps improve signal quality and reduce crosstalk, especially between CLK signals and other signals.

- Design the trace length of SDIO_TF_DAT [0:3] and SDIO_TF_CMD based on the trace length of SDIO_TF_CLK, and ensure that the deviation falls within ±500 mils.
- The impedance of trace is 50Ω.
- The total trace length cannot exceed 3 inches.

2.6 Low Speed Interface

2.6.1 I2S

The RDK X5 Module provides 2 I2S interfaces.

- Two I2S interfaces support full-duplex and a maximum data rate of 40 Mbps in master mode.
- In RX mode, it supports 1/2/4/8/16-channel audio input.
- In TX mode, it supports 1/2-channel audio output.

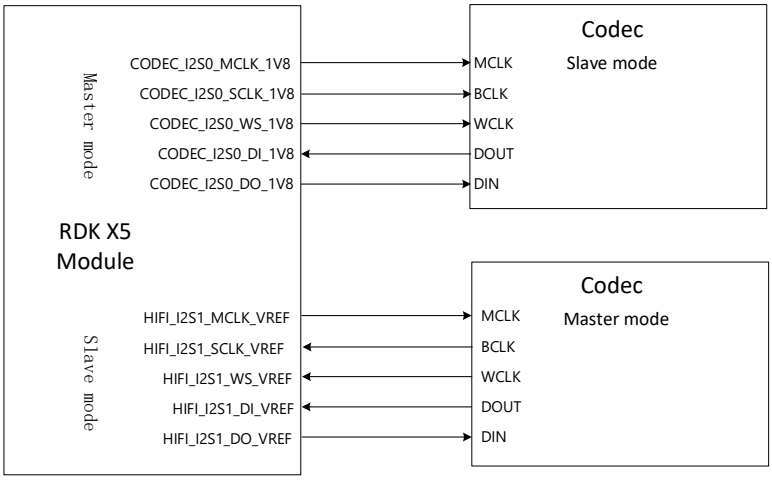
I2S interface includes the following pins.

MD Pin No.	Signal Name	Description
236	CODEC_I2S0_DO_1V8	GPIO: Data Output line for the I2S0.
238	CODEC_I2S0_SCLK_1V8	GPIO: Serial clock signal for the I2S0.
240	CODEC_I2S0_WS_1V8	GPIO: Word Select signal for the I2S0.
242	CODEC_I2S0_DI_1V8	GPIO: Data Input line for the I2S0.
246	CODEC_I2S0_MCLK_1V8	GPIO: Master Clock signal for the I2S0.
25	HIFI_I2S1_DO_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
26	HIFI_I2S1_WS_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
27	HIFI_I2S1_DI_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
49	HIFI_I2S1_SCLK_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
54	HIFI_I2S1_MCLK_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.

NOTE:

1. I2S0 operates with a 1.8V voltage level, while I2S1 supports the switching between two voltage levels of 1.8V and 3.3V.
2. Only I2S0 can be used in sleep mode. If need to support voice wake-up, please use I2S0 to connect the audio codec.

Refer to follow figure for the connecting of I2S interface design.



2.6.2 PDM

The RDK X5 Module provides two channel PDM interfaces, which can meet the input requirements of digital microphones.

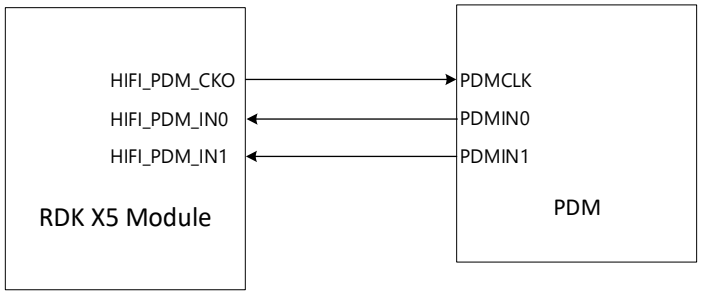
PDM interface includes the following pins.

MD Pin No.	Signal Name	Description
21	LED_SYS_STATUS_1V8	IO Multiplex: DSP_PDM_CKO
89	HOST_DIS_WLAN_N_1V8	IO Multiplex: DSP_PDM_IN1 Internal 10KΩ pull-up to VDDIO18_DSP_UART.
91	HOST_DIS_BT_N_1V8	IO Multiplex: DSP_PDM_IN0 Internal 10KΩ pull-up to VDDIO18_DSP_UART.

NOTE:

1. On the RDK X5 Module, these functions are multiplexed with other GPIO functions and need to be switched through software configuration.

Refer to follow figure for the connecting of PDM interface design.



2.6.3 SPI

The RDK X5 Module integrates up to four SPI interfaces.

- The SPI interfaces support both master mode and slave mode.
- In master mode, the maximum data rate is 50 Mbps.

- In slave mode, the maximum data rate is 32 Mbps.
- SPI1 supports 2 chip-select signals.

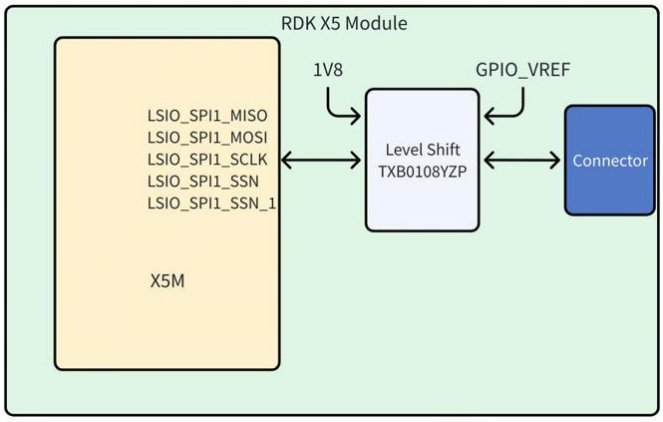
SPI interface includes the following pins.

MD Pin No.	Signal Name	Description
37	LSIO_SPI1_SSN0_JTAG_TRSTN_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
38	LSIO_SPI1_SCLK_JTAG_TCK_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
39	LSIO_SPI1_SSN1_JTAG_TMS_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
40	LSIO_SPI1_MISO_JTAG_TDI_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
44	LSIO_SPI1_MOSI_JTAG_TDO_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
24	LSIO_SPI2_MISO_PWM2_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
30	LSIO_SPI2_CS_PWM1_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
34	LSIO_SPI2_SCLK_PWM0_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
45	LSIO_SPI2_MOSI_PWM3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
70	CAM1_MCLK_1V8	IO Multiplex: LSIO_SPI3_SCLK.
72	CAM2_MCLK_1V8	IO Multiplex: LSIO_SPI3_SSN.
237	CAM3_MCLK_1V8	IO Multiplex: LSIO_SPI3_MISO.
239	CAM4_MCLK_1V8	IO Multiplex: LSIO_SPI3_MOSI.
203	CAN_SPI5_MISO	GPIO: SPI5 Master In Slave Out, default for CAN controllers and transceivers on the RDK X5 Module Carrier Board.
204	CAN_SPI5_CS	GPIO: SPI5 Chip Select, default for CAN controllers and transceivers on the RDK X5 Module Carrier Board.

MD Pin No.	Signal Name	Description
205	CAN_SPI5_MOSI	GPIO: SPI5 Master Out Slave In, default for CAN controllers and transceivers on the RDK X5 Module Carrier Board.
206	CAN_SPI5_SCLK	GPIO: SPI5 Serial Clock, default for CAN controllers and transceivers on the RDK X5 Module Carrier Board.

NOTE:

1. Due to the constraints of the level shifter IC (TXB0108YZP) on the Module, it is not recommended to add external pull-up or pull-down resistors to the SPI1 signals. If mandatory, it is recommended the value should be larger than 50KΩ. It is recommended to consult the TXB0108YZP datasheet for further details.



2. The voltage level of SPI5 is 1.8V.

2.6.3.1 SPI PCB Design

The design requirements on the SPI signals are as follows:

- Avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. If possible, route the SPI on inner layers to avoid EMI emission.
- Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule. It is recommended that the distance between the SCLK signal and other signals (including MISO and MOSI signal) can be 3W or more.
- The signal trace length should be as short as possible.
- If used a low frequency SCLK, SPI signal traces could be set lower priority than other critical signals.

2.6.4 I2C

The RDK X5 Module provides 7 I2C interfaces for customized design, while there are total 8 I2C interfaces in X5 SoC.

- Only I2C4 supports a data rate of 3.4 Mbps, while I2C0, I2C1, I2C2, I2C3, I2C5, and I2C6 only support up to 400 KHz and the SMBus protocol.
- I2C2 is a dedicated interface for the platform's PMIC and is not used as an interface for peripheral

devices.

I2C interface includes the following pins.

MD Pin No.	Signal Name	Description
35	LSIO_SCL0_PWM4_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2KΩ pull-up to GPIO_VREF.
36	LSIO_SDA0_PWM5_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2KΩ pull-up to GPIO_VREF.
28	LSIO_SDA1_PWM7_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 2KΩ pull-up to GPIO_VREF.
31	LSIO_ SCL1_PWM6_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 2KΩ pull-up to GPIO_VREF.
80	LSIO_SCL3_3V3	GPIO: I2C for Fan controller and Display on the Carrier Board. Internal 10KΩ pull-up to MD_3.3V.
82	LSIO_SDA3_3V3	GPIO: I2C for Fan controller and Display on the Carrier Board. Internal 10KΩ pull-up to MD_3.3V.
225	CAM2_SDA4_1V8	GPIO: Camera2 I2C bus on RDK X5 Module, no pull-up resisters on the Module.
227	CAM2_SCL4_1V8	GPIO: Camera2 I2C bus on RDK X5 Module, no pull-up resisters on the Module.
56	LSIO_SCL5_RX3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 1.8KΩ pull-up to GPIO_VREF.
58	LSIO_SDA5_TX3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 1.8KΩ pull-up to GPIO_VREF.
241	CAM1_SDA6_1V8	GPIO: Camera1 I2C bus on RDK X5 Module, no pull-up resisters on the Module.
243	CAM1_SCL6_1V8	GPIO: Camera1 I2C bus on RDK X5 Module, no pull-up resisters on the Module.
209	CODEC_HDMI_SCL7	GPIO: I2C7_SCL. It is used as I2C for HDMI transmitter (located on the Module, I2C address: 0x76). Internal 2KΩ pull-up to MD_1.8V.
211	CODEC_HDMI_SDA7	GPIO: I2C7_SDA. It is used as I2C for HDMI transmitter (located on the Module, I2C address: 0x76). Internal 2KΩ pull-up to MD_1.8V.

NOTE:

1. With the default software driver, I2C2 and I2C6 are utilized as the I2C control buses for two

cameras. I2C3 serves as the camera I2C bus with 3.3V digital logic.

2. Pay attention to the equivalent pull-up resistors in the entire signal chain, to avoid too small pull-up resistance resulting in signal levels that do not meet requirements.

2.6.5 UART

The RDK X5 Module provides 6 UART interfaces for customized design, while there are total 8 UART interfaces in X5 chip.

- UART0 is dedicated for system debugging and operates at a baud rate of 921600 bps.
- UART5 is dedicated to the onboard Bluetooth and Wi-Fi modules and cannot be used for other devices.
- UART1, UART2, UART3, UART4, UART6, and UART7 support baud rates of 9600, 38400, 57600, 921600, 115200, and 4M.
- UART2, UART3, UART4, UART5, and UART6 support the standard mode.
- UART7 supports the auto-flow control mode.

UART interface includes the following pins.

MD Pin No.	Signal Name	Description
64	DEBUG_UART0_TXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.
68	DEBUG_UART0_RXD_1V8	X5 SoC dedicated serial port. Must be connected for debugging and software burning.
51	LSIO_UART1_RX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
55	LSIO_UART1_TX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
41	LSIO_UART2_RX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
46	LSIO_UART2_TX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
56	LSIO_SCL5_RX3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 1.8KΩ pull-up to GPIO_VREF.
58	LSIO_SDA5_TX3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 1.8KΩ pull-up to GPIO_VREF.
215	LSIO_UART4_RXD_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
217	LSIO_UART4_TXD_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
29	LSIO_UART7_CTS_N_VREF	IO Multiplex: LSIO_UART6_RXD. GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.

MD Pin No.	Signal Name	Description
47	LSIO_UART7_RTS_N_VREF	IO Multiplex: LSIO_UART6_TXD. GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
29	LSIO_UART7_CTS_N_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
47	LSIO_UART7_RTS_N_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
48	LSIO_UART7_RX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
50	LSIO_UART7_TX_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.

NOTE:

1. The Pin names of the UART (TX&RX) are from the view of X5 SoC. For example, UART1_TXD is a transmitting signal and output from X5 SoC, meanwhile UART1_RXD is a receiving signal and input to X5 SoC.
2. If DEBUG_UART0 (Pin64, Pin68) need to be pulled up, the pull-up power supply must to use VDDIO18_DSP_UART (Pin231).
3. Pay attention to the equivalent pull-up resistors in the entire signal chain, to avoid too small pull-up resistance resulting in signal levels that do not meet requirements.

2.6.6 PWM

The RDK X5 Module supports 8 PWM interfaces.

- The frequency of the output waveform is programmable, ranging from 0.05Hz to 1MHz.
- It also provides a reference mode and can output waveforms with various duty cycles.

MD Pin No.	Signal Name	Description
34	LSIO_SPI2_SCLK_PWM0_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
30	LSIO_SPI2_CS_PWM1_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
24	LSIO_SPI2_MISO_PWM2_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
45	LSIO_SPI2_MOSI_PWM3_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V.
35	LSIO_SCL0_PWM4_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2KΩ pull-up to GPIO_VREF.

MD Pin No.	Signal Name	Description
36	LSIO_SDA0_PWM5_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2KΩ pull-up to GPIO_VREF.
31	LSIO_ SCL1_PWM6_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 2KΩ pull-up to GPIO_VREF.
28	LSIO_SDA1_PWM7_VREF	GPIO: typically 3.3V voltage level. Can be change to 1.8V voltage level by connecting GPIO_VREF to MD_1.8V. Internal 2KΩ pull-up to GPIO_VREF.

2.6.6.1 PWM PCB Design

The design requirements on the PWM signals are as follows:

- For high frequency PWM design, avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule.

2.6.7 LPWM

RDK X5 Module provides 8 channels of LPWM signal.

- The frequency of the output pulse is programmable, ranging from 1Hz to 1MHz.
- The width of the pulse is programmable, ranging from 1μs to 4ms.
- It supports generating output pulses with multiple trigger sources, such as PPS, EMAC, and the internal system timer.

MD Pin No.	Signal Name	Description
206	CAN_SPI5_SCLK	IO Multiplex: LSIO_LPWM_IO0
204	CAN_SPI5_CS	IO Multiplex: LSIO_LPWM_IO1
203	CAN_SPI5_MISO	IO Multiplex: LSIO_LPWM_IO2
205	CAN_SPI5_MOSI	IO Multiplex: LSIO_LPWM_IO3
70	CAM1_MCLK_1V8	IO Multiplex: LSIO_LPWM_IO4
72	CAM2_MCLK_1V8	IO Multiplex: LSIO_LPWM_IO5
237	CAM3_MCLK_1V8	IO Multiplex: LSIO_LPWM_IO6
239	CAM4_MCLK_1V8	IO Multiplex: LSIO_LPWM_IO7

NOTE:

1. When LPWM is used for synchronization between multiple cameras, the same group of LPWM should be used, where LPWM0/1/2/3 is a group and LPWM4/5/6/7 is a group. In other words, when multiple cameras need to be synchronized, the synchronization signals they use cannot be in two different groups.

2.6.7.1 LPWM PCB Design

The design requirements on the LPWM signals are as follows:

- For high frequency LPWM design, avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule.

2.6.8 MCLK

The RDK X5 Module provides four channels of MCLK signals, which can be used to drive the camera module.

MD Pin No.	Signal Name	Description
70	CAM1_MCLK_1V8	IO Multiplex: LSIO_SENSOR0_MCLK
72	CAM2_MCLK_1V8	IO Multiplex: LSIO_SENSOR1_MCLK
237	CAM3_MCLK_1V8	IO Multiplex: LSIO_SENSOR2_MCLK
239	CAM4_MCLK_1V8	IO Multiplex: LSIO_SENSOR3_MCLK

2.6.9 ADC

The RDK X5 Module has 4 ADCs.

- ADC7 is used for the hardware identification of the carrier board, which facilitates customers to distinguish the board ID.
- The other 3 ADCs can be used for various types of data collection and voltage monitoring.

MD Pin No.	Signal Name	Description
210	ADC_VINS4	The 4th ADC input channel, maximum input voltage of 1.8V
212	ADC_VINS3	The 3rd ADC input channel, maximum input voltage of 1.8V
216	ADC_VINS7_RSVD	The 7th ADC input channel, maximum input voltage of 1.8V.
218	ADC_VINS5	The 5th ADC input channel, maximum input voltage of 1.8V

NOTE:

1. In practical applications, it is recommended that the ADC's sampling voltage range be maintained between approximately 100mV and 1700mV, as this helps improve the sampling accuracy of the ADC. Additionally, configuring an appropriate operating mode and sampling rate through software can help achieve a balance between accuracy and resource utilization.

2.7 PIN Delay

D-Robotics recommends that customers control the delay of high-speed signals and pay attention to the impact of PCB material and routing form on signal speed during the process. The Pin Delay sheet of ***RDK X5 Module Pinout Description and Application Note*** shows the pin delay data on the RDK X5 Module.

NOTE:

When routing *MIPI CSI signals*, must import the pin delay data. *Due to the limitation of board*

size, MIPI CSI signals are not strictly controlled in equal length on the module.

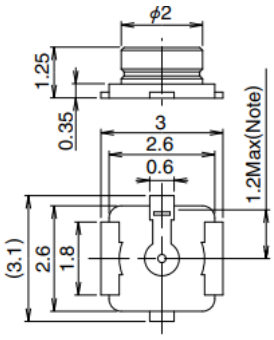
2.8 Wireless Connectivity

The RDK X5 module can be optionally equipped with a dual-band 2.4/5GHz wireless module (FCS960K), supports Wi-Fi 6 protocol and Bluetooth 5.4 protocol.

- Compliant with IEEE 802.11a/b/g/n/ac/ax protocols.
- WIFI and Bluetooth share one antenna.

NOTE:

1. The IPEX part number is U.FL-R-SMT-1(80) from Hirose Electric.



U.FL-R-SMT-1

Due to limitations in the number of available hardware interfaces, the UART for Bluetooth on the Module lacks hardware flow control (RTS/CTS). As a result, not all Bluetooth features can be implemented. Only basic functions can be supported, such as AT command interaction and data transmission without real-time requirements.

3 Mechanical

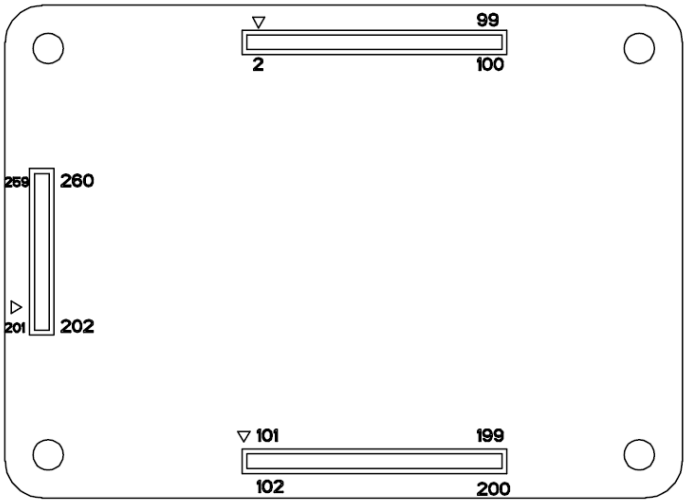
3.1 Connectors

The three connectors have two specifications. Except for the total number of pins, the parameters of the other connectors are the same.

The part number of the connectors on the RDK X5 Module are listed below. Customers can choose the appropriate stacking height of the connector on Carrier Board according to the product form.

No. of Contacts	Header on Module	Mfr.	Stacking height	Receptacle on Carrier Board
100 Pins	DF40C-100DP-0.4V(51)	HRS	1.5mm	DF40C-100DS-0.4V(51)
			3.0mm	DF40HC(3.0)-100DS-0.4V(51)
60 Pins	DF40C-60DP-0.4V(51)	HRS	1.5mm	DF40C-60DS-0.4V(51)
			3.0mm	DF40HC(3.0)-60DS-0.4V(51)

The RDK X5 module Connector PIN sequence as below (bottom view).

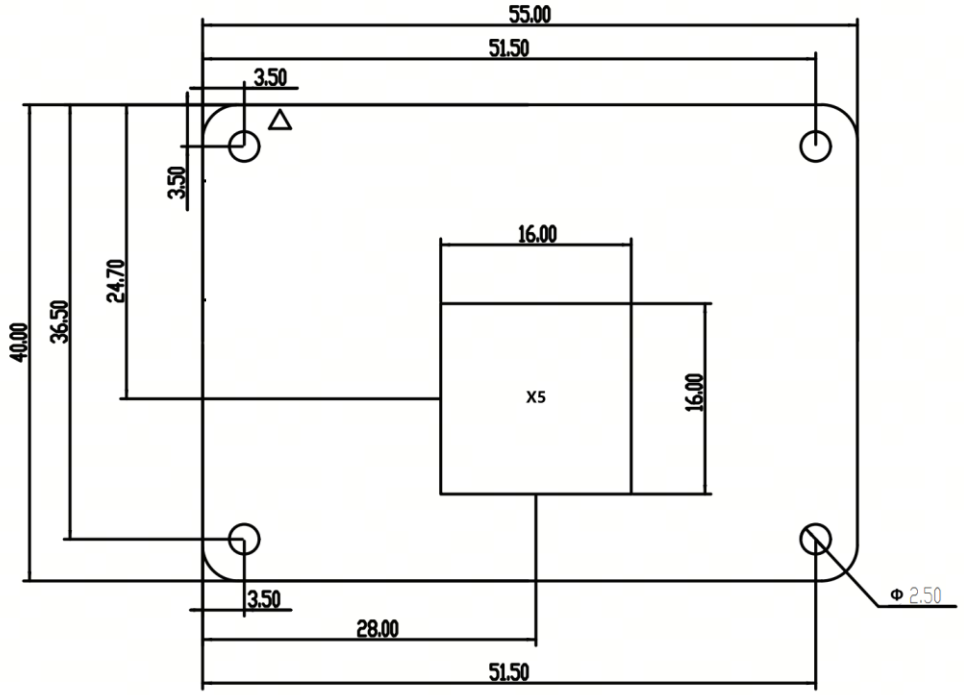


NOTE:

The four screw holes on the RDK X5 Module are not connected to the ground signal.

3.2 Structural dimensions

As shown in the figure below, these are the key structural dimensions of the RDK X5 Module.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24.70
36.50
40.00
X5
16.00
3.50
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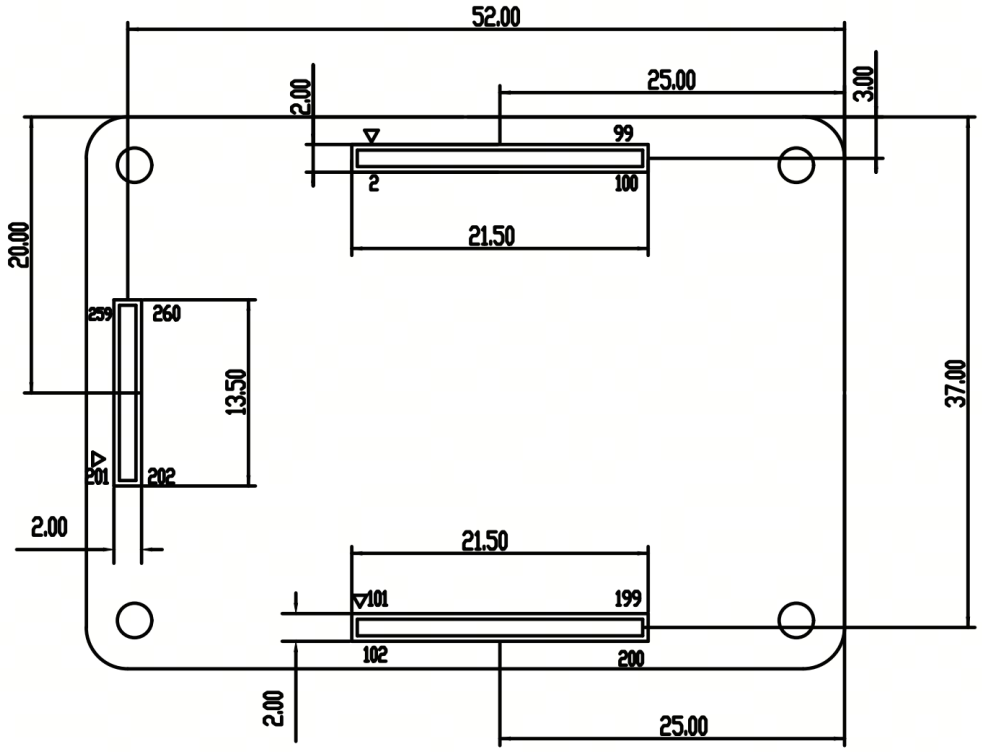
51.50
Φ 2.50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